In the Claims:

1. (currently amended) A system comprising:

shared system registers, each register including one or more bits defining an access protocol, and one or more bits representing data; and

N processors, ~~n~~N≥2, where ~~n~~N is an integer, each accessing the registers~~:~~.

2. (currently amended) A system, as defined in claim 1, wherein said one or more bits defining the access protocol ~~including~~include one or more bits that define a ~~configurable~~ register access type for each N processors.

3. (currently amended) A system, as defined in claim 2, the register access type being selected from a group that includes READ, READ/CLEAR, READ/SET, and READ/WRITE.

4. (currently amended) A system, as defined in claim 3, further comprising at least one programmable configuration registers operative to encode and store said one or more bits defining the access protocol, each configuration register corresponding to one of the shared system registers.

5. (original) A system, as defined in claim 4, wherein:

each programmable configuration register consisting of N*2 bits; and

the configurable access types are encoded into 2 bits.

6. (currently amended) A system, as defined in claim 3, the access protocol encoded and provided as input signals to the hardware design.

7. (original) A system, as defined in claim 3, the access protocol encoded and selected as a build-time option in the hardware design source code.

8. (original) A system, as defined in claim 3, the access protocol further including an arbitration priority.

9. (currently amended) A system, as defined in claim 8, comprising programmable configuration registers operative to encode and store the access protocol, each configuration register corresponding to one of the shared system registers.

10. (original) A system, as defined in claim 9, wherein:

N is 2; and

each programmable register including 5-bits, 2 bits represent the access type of one of the two processors, 2 bits represent the access type of the other of the two processors, and 1 bit represents the arbitration priority.

11. (original) A system, as defined in claim 9, wherein:

each programmable configuration registers consists of N*(2+ceiling(log2 N)) bits; and

the access protocol including the four access types are encoded into 2 bits per processor and the arbitration priority encoded into ceiling(log, N) bits.

12. (original) A system, as defined in claim 8, the access protocol encoded and selected as a build-time option in the hardware design source code.

13. (currently amended) A system, as defined in claim 8, the access protocol encoded and provided as input signals to the hardware design.